MPIB63S-68KX3
(PC-133 256MB 168pin Registered SDRAM DIMM)

DESCRIPTION

The MPIB63S-68KX3 is 32M bit x 72 Synchronous Dynamic RAM high density memory module. The MPIB63S-68KX3 consists of eighteen CMOS 16M x 8 bit with 4 banks Synchronous DRAMs in TinyBGA package, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The MPIB63S-68KX3 is a Dual in-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system application.

FEATURES

- Performance range – 133Mhz Max. Freq. (CL=3)
- Burst mode operation
- Auto & self-refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- MRS cycle with address key programs
- Latency (Access from column address)
- Burst Length (1, 2, 4, 8 & Full page)
- Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB: Height (1200 mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Back	Pin	Back
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	/CS2	87	DQ33	129	/CS3
4	DQ2	46	DQM2	88	DQ34	130	DQM6
5	DQ3	47	DQM3	89	DQ35	131	DQM7
6	V_{DD}	48	DU	90	V_{DD}	132	*A13
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	*V_{REF}	104	DQ47	146	*V_{REF}
21	CB0	63	CKE1	105	CB4	147	REGE
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	/CS0	72	DQ27	114	/CS1	156	DQ59
31	DU	73	V_{DD}	115	/RAS	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	**SA0
40	V_{DD}	82	**SDA	124	V_{DD}	166	**SA1
41	V_{DD}	83	**SCL	125	CLK1	167	**SA2
42	CLK0	84	V_{DD}	126	*A12	168	V_{DD}

PIN NAME

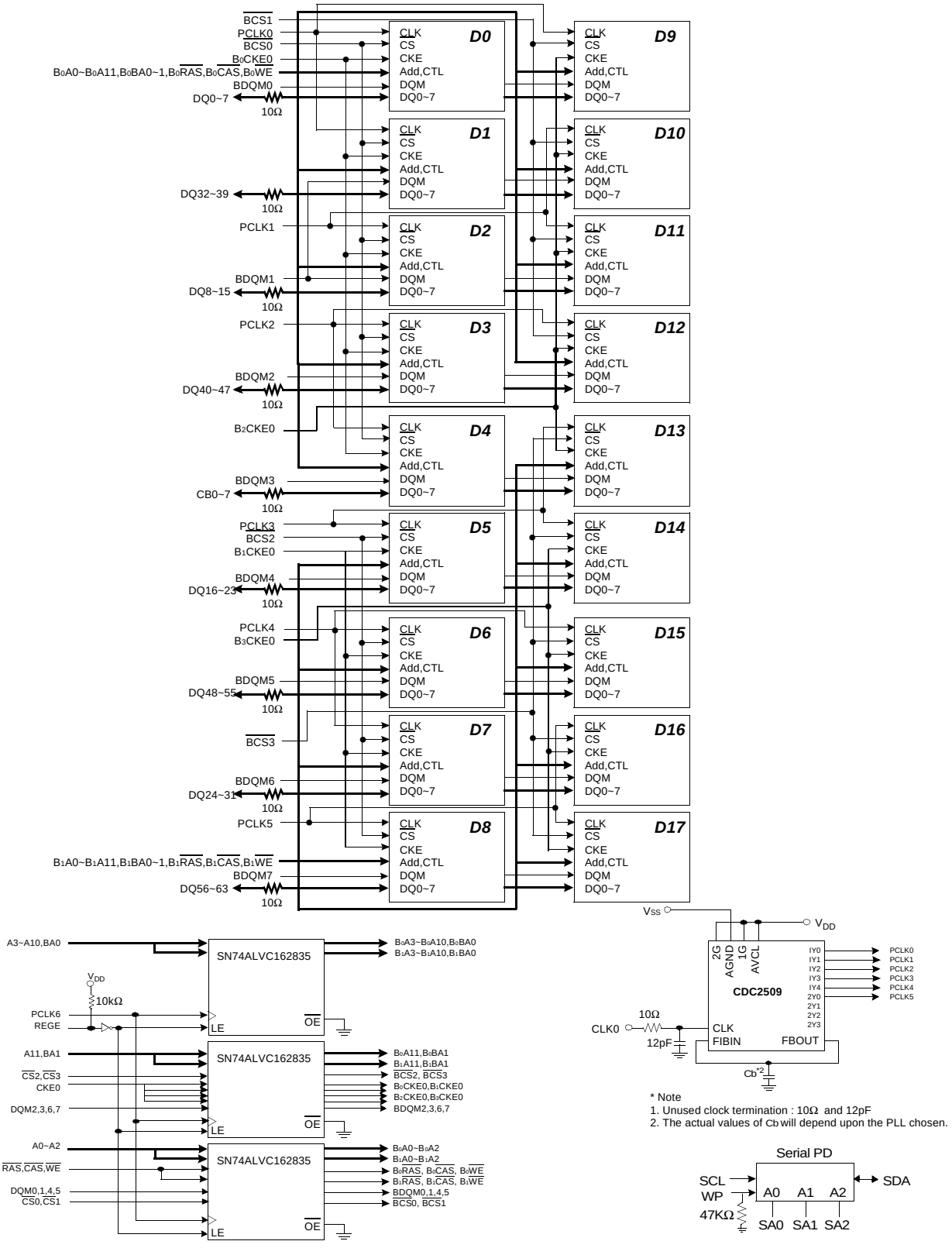
Pin Name	Function
A0~A12	Address input (Multiplexed)
BA0~BA1	Select bank
DQ0~DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0~CLK3	Clock input
CKE0~CKE1	Clock enable input
/CS0~/CS3	Chip select input
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
DQM0~7	DQM
V_{DD}	Power supply (3.3V)
V_{SS}	Ground
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
/CS	*Chip select*	Disables or enables device operation by masking or enabling al inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1 CLK+t_{SS} prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address: RA0 ~RA11, Column address: CA0 ~CA9
BA0 ~ BA1	*Bank select address*	Selects bank too be activated during row address latch time. Select bank for read/write during column address latch time.
/RAS	*Row address strobe*	Latches row address on the positive going edge of the CLK with /RAS low. Enable row access & precharge.
/CAS	*Column address strobe*	Latches column address on the positive going edge of the CLK with /CAS low. Enable column access.
/WE	*Write enable*	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.(Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the address and control inputs are latched if CLK is held at a high or low logic level. The inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Register on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data input/output are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to VSS through 47K ohm Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.


BCS1
PCLK0
BCS0
B0CKE0
B0A0~B0A11,B0BA0~1,B0RAS,B0CAS,B0WE
BDQM0
DQ0~7
10Ω
DQ32~39
PCLK1
BDQM1
DQ8~15
PCLK2
BDQM2
DQ40~47
B2CKE0
BDQM3
CB0~7
PCLK3
BCS2
B1CKE0
BDQM4
DQ16~23
PCLK4
B3CKE0
BDQM5
DQ48~55
BCS3
BDQM6
DQ24~31
PCLK5
B1A0~B1A11,B1BA0~1,B1RAS,B1CAS,B1WE
BDQM7
DQ56~63
CLK
CS
CKE
Add,CTL
DQM
DQ0~7
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
A3~A10,BA0
SN74ALVC162835
B0A3~B0A10,B0BA0
B1A3~B1A10,B1BA0
VDD
10kΩ
PCLK6
REGE
LE
OE
A11,BA1
B0A11,B0BA1
B1A11,B1BA1
CS2,CS3
CKE0
B0CKE0,B1CKE0
B2CKE0,B3CKE0
DQM2,3,6,7
BDQM2,3,6,7
A0~A2
RAS,CAS,WE
B0A0~B0A2
B1A0~B1A2
B0RAS, B0CAS, B0WE
B1RAS, B1CAS, B1WE
DQM0,1,4,5
CS0,CS1
BDQM0,1,4,5
BCS0, BCS1
VSS
VDD
2G
AGND
1G
AVCL
CDC2509
IY0
IY1
IY2
IY3
IY4
2Y0
2Y1
2Y2
2Y3
PCLK0
PCLK1
PCLK2
PCLK3
PCLK4
PCLK5
CLK0
10Ω
12pF
CLK
FIBIN
FBOUT
Cb*2
* Note
1. Unused clock termination : 10Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.
Serial PD
SCL
WP
47KΩ
A0
A1
A2
SDA
SA0
SA1
SA2

ABSOLUTE MAXIMUM RATIINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +125	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RANTINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC OPERATING CONDITIONS AND CHARACTERISTIICS

Recommended operating conditions(Voltage referenced to VSS = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note : 1. VIH (max) = 5.6V AC. The overshoot voltage duration is ≤ 5ns

2. VIL (min) = -2.0V AC. The undershoot voltage duration is ≤ 5ns

3. Any input 0V ≤ VIN ≤ VDDQ.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	-	8	pF
/RAS, /CAS, /WE	C_{IN}	-	8	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	-	8	pF
Clock (CLK0 ~ CLK1)	C_{CLK}	-	6	pF
/CS (/CS0 ~ /CS1)	C_{CS}	-	8	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	-	8	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	-	8	pF
REGE	C_{REGE}	-	5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C) (Note: 1, 2, 3, 4)

Parameter/Condition		Symbol	Max	Unit	Note
OPERATING CURRENT: Active Mode; Burst = 2; READ or WEITE; t_{RC} = t_{RC} (MIN); CAS latency = 3		I_{DD1}	1,800	mA	5, 6, 7, 8
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		I_{DD2}	36	mA	8
STANDBY CURRENT: Active Mode; S0#, S1# = HIGH; CKE = HIGH; All banks active after t_{RCD} met; No access in progress		I_{DD3}	900	mA	5, 7, 8, 9
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		I_{DD4}	1,800	mA	5, 6, 7, 8
AUTO REFRESH CURRENT: CKE = HIGH; S0# = HIGH;	t_{RC}= t_{RC}(MIN); CL = 3	I_{DD5}	3,240	mA	5, 6, 7, 8, 10, 12
	t_{RC} = 15.325µs; CL = 3	I_{DD6}	54	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}	36	mA	11

Note: 1. All voltage referenced to V_{SS}.

2. An initial pause of 100µs is required after power-down, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously, V_{SS} and V_{SSQ} must be at the same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.

3. AC timing and IDD tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to the 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crossover point.

4. I_{DD} specifications are tested after the device is properly initialized.

5. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.

6. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.

7. Address transitions average one transition every two clocks.

8. t_{CK} = 7.5ns.

9. Other input signals are allowed to transition no more than once every two clocks and ate otherwise at valid V_{IH} or V_{IL} levels.

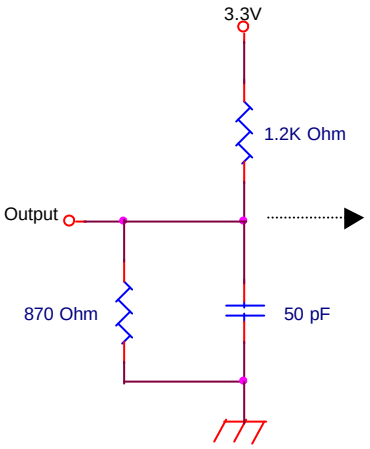
10. CKE is HIGH refresh command period (t_{RFC} [Min]) else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.

11. Enables on-chip refresh and address counters.

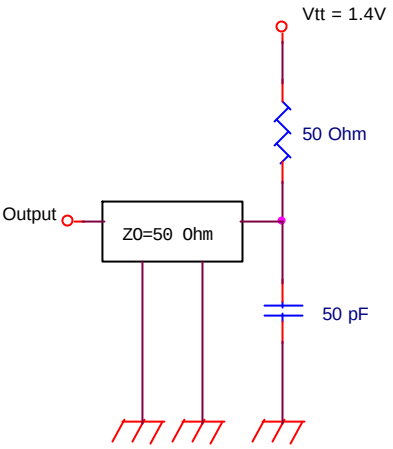
12. Other input signals ate allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.1	V
Input rise and fall time	tr/tf = 1/1	Ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



V_{OH}(DC) = 2.4V
I_{OH} = -2mA
V_{OL}(DC) = 0.4V
I_{OL} = 2mA



(Fig.1) DC output load circuit

(Fig.2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
Row active to row active delay	t_{RRD}(min)	15	ns	1
/RAS to /CAS delay	t_{RCD}(min)	20	ns	1
Row precharge time	t_{RP}(min)	20	ns	1
Row active time	t_{RAS}(min)	44	ns	1
	t_{RAS}(max)	120	us	
Row cycle time	t_{RC}(min)	66	ns	1
Last data in to row precharge	t_{RDL}(min)	2	CLK	2, 5
Last data in to Active delay	t_{DAL}(min)	2 CLK + 20ns	-	5
Last data in to new col. Address delay	t_{CDL}(min)	1	CLK	2
Last data in to burst stop	t_{BDL}(min)	1	CLK	2
Col. Address to col. Address delay	t_{CCD}(min)	1	CLK	3
Number of valid output data	CAS latency = 3	2	ea	4
	CAS latency = 2	1		

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and Then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and teas burst stop.

5. t_{RDL} = 1 CLK and t_{DAL} = 1 CLK + 20 ns is also support.
Kingmax recommends t_{RDL} = 2 CLK and t_{DAL} = 2 CLK + 20 ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE

Parameter		Symbol	100MHz		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	ns	1
	CAS latency=2		10			
CLK to valid output delay	CAS latency=3	t_{SAC}		5.4	ns	1, 2
	CAS latency=2			6		
Output data hold time	CAS latency=3	t_{OH}	2.7		ns	2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	2.5		ns	3
CLK low pulse width		t_{CL}	2.5		ns	3
Input setup time		t_{SS}	1.5		ns	3
Input hold time		t_{SH}	0.8		ns	3
CLK to output in Low-Z		t_{SLZ}	0.8		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		5.4	ns	
	CAS latency=2			6		

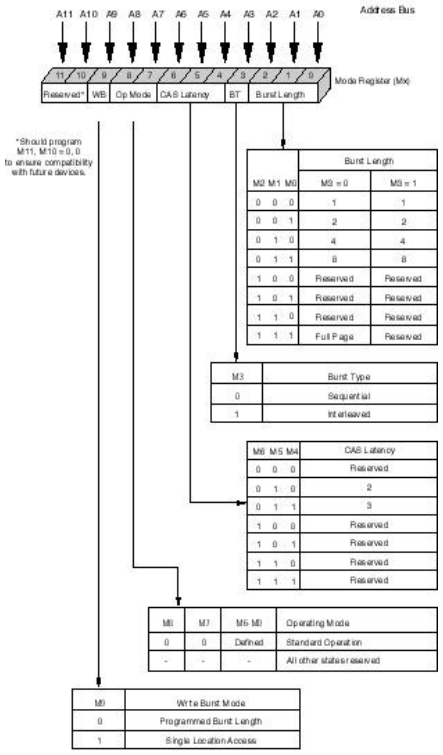
Note: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.

If tr & tf is longer than 1ns, transient time compensation should be considered,

i.e., [(tr + tf)/2-1]ns should be added to the parameter.



MODE REGISTER DEFINITION

BURST DEFINITION

Burst length	Starting Col. addr.			Order of access within a burst	
				Type=Sequential	Type=Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (1,024)	n=A0-A9 (location 0-1,023)			$C_n, C_{n+1}, C_{n+2}, C_{n+3}, C_{n+4}$ ……$_n$C$_n$-1,C_n	Not supported

Note: 1. For a burst length of two, A1-A9 select the block of two Burst ; A0 selects the starting column within the block.

2. For a burst length of four, A2-A9 select the block of four burst; A0-A1 select the starting column within the block.

3. For a burst length of eight, A3-A9 select the block of four burst; A0-A2 select the starting column within the block.

4. For a full page burst, the full row is selected and A0-A9 select the starting column.

5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

6. For a burst length of one, A0-A9 select the unique column to be accessed and Mode Register bit M3 is ignored.

SIMPLIFIED TRUTH TABLE

Command			CKE_{n-1}	CKE_n	/CS	/RAS	/CAS	/WE	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9~A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1, 2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row address			H	X	L	L	H	H	X	V	Row address		
Read & Col. addr.	Auto precharge disable		H	X	L	H	L	H	X	V	L	Col. Addr.	4
	Auto precharge enable										H	(A_0~A_9)	4, 5
Write & Col. addr.	Auto precharge disable		H	X	L	H	L	L	X	V	L	Col. Addr.	4
	Auto precharge enable										H	(A_0~A_9)	4, 5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid, X = Don't care, H = Logic high, L = logic low)

Note: 1. OP Code: Operand code

A_0 ~ A_{11} & BA_0 ~ BA_1: Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatic precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1: Bank select addresses.

If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.

If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks ate selected.

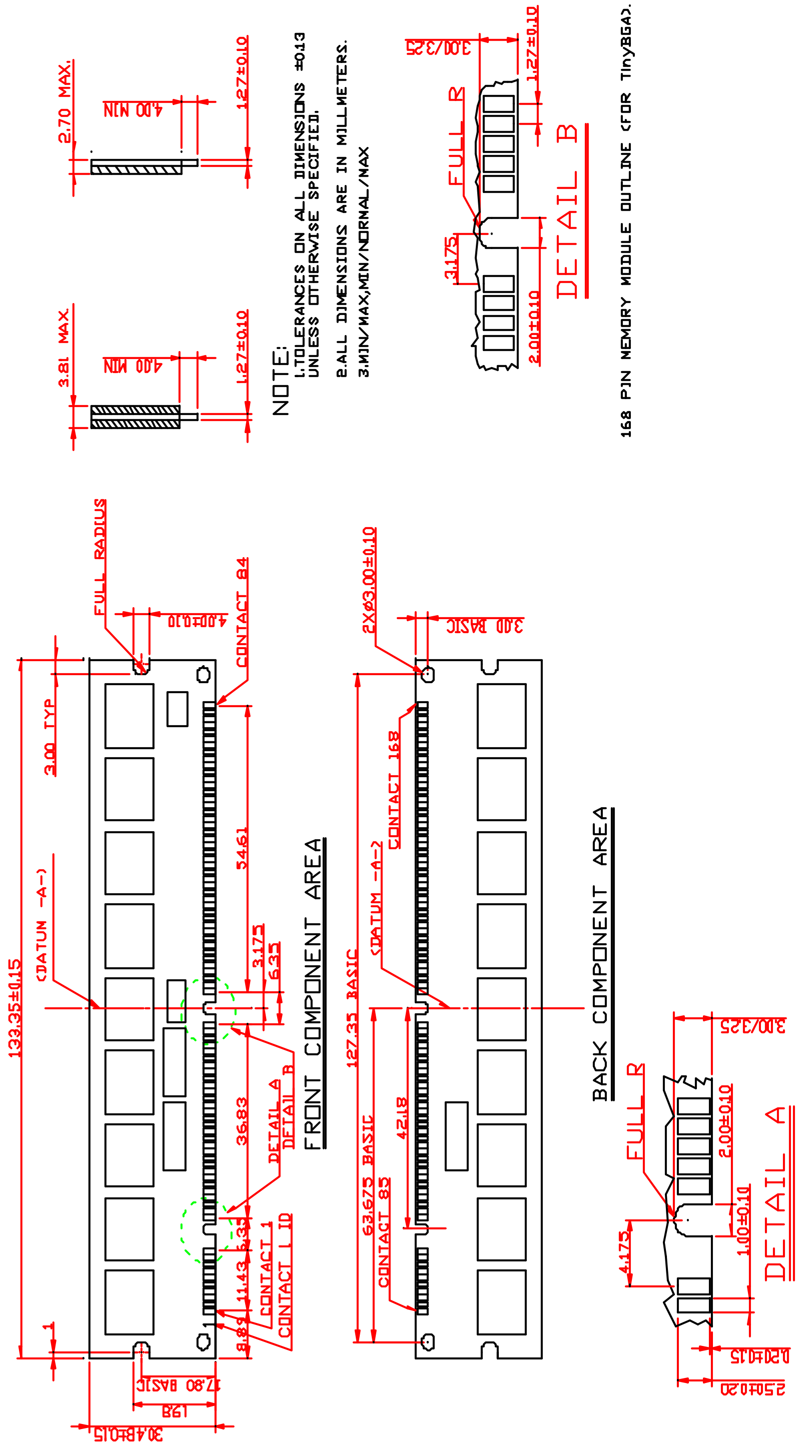
5. During burst read or write with auto prechatge, new read/write command can not be issued.

Another bank read/write command can issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)


NOTE:
1.TOLERANCES ON ALL DIMENSIONS ±0.13 UNLESS OTHERWISE SPECIFIED.
2.ALL DIMENSIONS ARE IN MILLMETERS.
3.MIN/MAX,MIN/NORMAL/MAX
168 PIN MEMORY MODULE OUTLINE (FOR TinyBGA).
FRONT COMPONENT AREA
BACK COMPONENT AREA
DETAIL A
DETAIL B
FULL R
FULL RADIUS
CONTACT 84
CONTACT 85
CONTACT 168
CONTACT 1
133.35±0.15
127.35 BASIC
63.675 BASIC
54.61
36.83
42.18
3.00 TYP
3.00 BASIC
2XØ3.00±0.10
4.00±0.10
2.70 MAX.
3.81 MAX.
4.00 MIN
1.27±0.10
2.00±0.10
3.00/3.25
3.175
6.35
1.00±0.10
4.175